|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 0000/0001/0010 | ALU Operations | 0011 | LHI | 0100 | LOAD |
| |  | | --- | | “111” A1RF  D1 MEMINS (A)  MEMINS (D) IR  D1 ALU  +1 ALU  S1  ALU T1 | |  | | T1 D3  “111” A3RF  I6 – 8  A1RF  I9 – 11  A2RF  D1 ALU  D2 ALU  S2  ALU T1 | |  | | I3 – 5 A3RF  S3  T1 D3RF | | | |  | | --- | | “111” A1RF  D1 MEMINS (A)  MEMINS (D) IR  D1 ALU  +1 ALU  S4  ALU T1 | |  | | T1 D3  S5  “111” A3RF | |  | | I0 – 8  SE9 – 16  LS7  LS7  D3RF  S6  I9 – 11  A3RF | | | |  | | --- | | “111” A1RF  D1 MEMINS (A)  MEMINS (D) IR  D1 ALU  +1 ALU  S7  ALU T1  S8 | |  | | T1 D3  “111” A3RF  I6 – 8  A1RF  D1 ALU  I0 – 5  SE6 – 16  ALU  ALU T1  S9 | |  | | T1 MEMDAT (A)  MEMDAT (DO) T2  S10 | |  | | T2 ALU  0 ALU  I9 – 11  A3RF  T2 D3RF | | |
|  | |  | |  | |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 0101 | STORE  S11 | 0110 | LOAD MULTIPLE  S14 | 0111 | STORE MULTIPLE  S18 |
| |  | | --- | | “111” A1RF  D1 MEMINS (A)  MEMINS (D) IR  D1 ALU  +1 ALU  ALU T1  S12 | |  | | T1 D3  “111” A3RF  I6 – 8  A1RF  D1 ALU  I0 – 5  SE6 – 16  ALU  ALU T1  S13 | |  | | I9 – 11  A2RF  T1 MEMDAT (A)  D2 MEMDAT(DI) | | | |  | | --- | | “111” A1RF  D1 MEMINS (A)  MEMINS (D) IR  D1 ALU  +1 ALU  ALU T1  S15 | |  | | T1 D3  “111” A3RF  I9-11  A2RF  D2 MEMDAT(A)  MEMDAT (DO) T2 | |  | | WHILE (PEINPUT IS VALID) {  T2 D3RF  PEOUTPUT A3RF  T2 ALU  +1 ALU  S16  ALU T1  S17 | |  | | T1 T2} | | | |  | | --- | | “111” A1RF  D1 MEMINS (A)  MEMINS (D) IR  D1 ALU  +1 ALU  ALU T1 | |  | | T1 D3  “111” A3RF  I9-11  A2RF  D2 MEMDAT(A), T2  PEOUTPUT  A1RF | |  | | WHILE (PEINPUT IS VALID) {  T2 MEMDAT(A)  D2MEMDAT(DI)  T2 ALU  +1 ALU  S20  ALU T1  S21 | |  | | PEOUTPUT  A1RF  T1 T2} |   S19 | |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 1100 | BEQ  S22 | 1000 | JAL  S26 | 1001 | JLR  S29 |
| |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | “111” A1RF  D1 MEMINS (A)  MEMINS (D) IR  D1 ALU  +1 ALU  ALU T1  S23 | | |  | |  | | | | | |  | I6 – 8  A1RF  I9 – 11  A2RF  D1 EQU  D2 EQU | | |  | | S24 | | | | | | T1 D3RF  “111” A3RF | |  | “111” A1RF  D1RF ALU  I0 – 5  SE6 – 16  ALU  ALU D3RF  “111” A3RF | | | | |  | | --- | | “111” A1RF  D1 MEMINS (A)  MEMINS (D) IR  D1 ALU  +1 ALU  ALU T1  S27 | |  | | T1 D3RF  I9-11 A3RF  “111” A1RF  D1RF ALU  I0 – 8  SE9 – 16  ALU  ALU T1 | |  | | T1 D3RF  “111” A3RF |   S28 | | |  | | --- | | “111” A1RF  D1 MEMINS (A)  MEMINS (D) IR  D1 ALU  +1 ALU  ALU T1  S30 | |  | | I9 – 11  A3RF  T1 D3RF  S31 | |  | | I6 – 8  A1RF  D1RF D3RF  “111” A3RF | | |

S25

# State Merging and Equivalence

//Note: S12 and S8 will require an additional signal from the Instruction Decoder. It differs from the other states in one input to the ALU. Can be modelled as a multiplexer. Also only S2 must cause a change in the flags. //

If a mealy machine is to be implemented, then that control signal can also be generated from the FSM. That can be decided over the weekend… The Data Path can also be edited suitably then.

This leaves us with about 16 states.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 0000/0001/0010 | ALU Operations | 0011 | LHI | 0100 | LOAD |
| |  | | --- | | “111” A1RF  D1 MEMINS (A)  MEMINS (D) IR  D1 ALU  +1 ALU  S1  ALU T1 | |  | | T1 D3  “111” A3RF  I6 – 8  A1RF  I9 – 11  A2RF  D1 ALU  D2 ALU  S2  ALU T1 | |  | | I3 – 5 A3RF  S3  T1 D3RF | | | |  | | --- | | “111” A1RF  D1 MEMINS (A)  MEMINS (D) IR  D1 ALU  +1 ALU  S1  ALU T1 | |  | | T1 D3  S2  “111” A3RF | |  | | I0 – 8  SE9 – 16  LS7  LS7  D3RF  S4  I9 – 11  A3RF | | | |  | | --- | | “111” A1RF  D1 MEMINS (A)  MEMINS (D) IR  D1 ALU  +1 ALU  S1  ALU T1  S2 | |  | | T1 D3  “111” A3RF  I6 – 8  A1RF  D1 ALU  I0 – 5  SE6 – 16  ALU  ALU T1  S5 | |  | | T1 MEMDAT (A)  MEMDAT (DO) T2  S6 | |  | | T2 ALU  0 ALU  I9 – 11  A3RF  T2 D3RF | | |
|  | |  | |  | |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 0101 | STORE  S1 | 0110 | LOAD MULTIPLE  S1 | 0111 | STORE MULTIPLE  S1 |
| |  | | --- | | “111” A1RF  D1 MEMINS (A)  MEMINS (D) IR  D1 ALU  +1 ALU  ALU T1  S2 | |  | | T1 D3  “111” A3RF  I6 – 8  A1RF  D1 ALU  I0 – 5  SE6 – 16  ALU  ALU T1  S7 | |  | | I9 – 11  A2RF  T1 MEMDAT (A)  D2 MEMDAT(DI) | | | |  | | --- | | “111” A1RF  D1 MEMINS (A)  MEMINS (D) IR  D1 ALU  +1 ALU  ALU T1  S8 | |  | | T1 D3  “111” A3RF  I9-11  A2RF  D2 MEMDAT(A)  MEMDAT (DO) T2 | |  | | WHILE (PEINPUT IS VALID) {  T2 D3RF  PEOUTPUT A3RF  T2 ALU  +1 ALU  S9  ALU T1  S10 | |  | | T1 T2} | | | |  | | --- | | “111” A1RF  D1 MEMINS (A)  MEMINS (D) IR  D1 ALU  +1 ALU  ALU T1 | |  | | T1 D3  “111” A3RF  I9-11  A2RF  D2 MEMDAT(A), T2  PEOUTPUT  A1RF | |  | | WHILE (PEINPUT IS VALID) {  T2 MEMDAT(A)  D2MEMDAT(DI)  T2 ALU  +1 ALU  S12  ALU T1  S10 | |  | | PEOUTPUT  A1RF  T1 T2} |   S11 | |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 1100 | BEQ  S1 | 1000 | JAL  S1 | 1001 | JLR  S1 |
| |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | “111” A1RF  D1 MEMINS (A)  MEMINS (D) IR  D1 ALU  +1 ALU  ALU T1  S13 | | |  | |  | | | | | |  | I6 – 8  A1RF  I9 – 11  A2RF  D1 EQU  D2 EQU | | |  | | S2 | | | | | | T1 D3RF  “111” A3RF | |  | “111” A1RF  D1RF ALU  I0 – 5  SE6 – 16  ALU  ALU D3RF  “111” A3RF | | | | |  | | --- | | “111” A1RF  D1 MEMINS (A)  MEMINS (D) IR  D1 ALU  +1 ALU  ALU T1  S15 | |  | | T1 D3RF  I9-11 A3RF  “111” A1RF  D1RF ALU  I0 – 8  SE9 – 16  ALU  ALU T1 | |  | | T1 D3RF  “111” A3RF |   S2 | | |  | | --- | | “111” A1RF  D1 MEMINS (A)  MEMINS (D) IR  D1 ALU  +1 ALU  ALU T1  S2 | |  | | I9 – 11  A3RF  T1 D3RF  S16 | |  | | I6 – 8  A1RF  D1RF D3RF  “111” A3RF | | |

S14